Proceedings of the 8th IEEE Mediterranean Conference
on Control and Automation (MED 2000)
Rio, Patras, GREECE 17-19 July, 2000

A LOW COST DIGITAL CURRENT TRANSDUCER

ALEXANDER PROSS

Nonlinear Systems Design Group, Priory Street,
Coventry University, CV1 5FB, United Kingdom, Email:pross2@gmx.de
Fax:+49 89 2443 43545, Fax-Voice Mail:+44 870 737 9000 5257,www.ligua.com

Abstract: This paper describes a Non-Hall effect current transducer, which provides galvanic isolation between the input and output whilst transmitting both ac an dc signals. The current transducer is used in electronic drives and controls systems where the special features of digital output and lack of Hall effect devices coupled with symmetrical magnetic structure is of benefit. The new design uses a ferrite core without an air gap, proving a limit cycle for the transmission of input signals. The limit cycle supports the production of a digital output signal.

Key Words: Transducers, Limit Cycle, Current Transducer, Digital Current Transducer

1. INTRODUCTION

Current Transducers are generally used for current measurement for electric drive system for which only a limited range of devices are available within normal commercial constraints. The transducer developed does not use a Hall effect device but rather a new method [1,2]. An extension of this technique provides a digital transducer, Fig. 1 with an output in the form previously published [2,3]. The transducer works on the same principle as the analogue transducer in that it uses a simple eliminatory filter based on a up/down counter. The digital transducer uses the same circuit structure as the analogue transducer but an additional Zero Order Hold was introduced which produces a sampled signal.

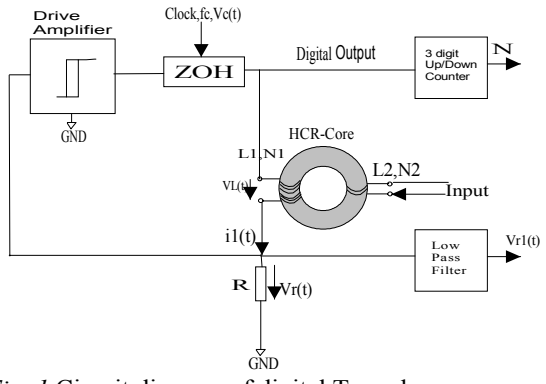

Fig. 1 Circuit diagram of digital Transducers

The sampling frequency (fc) was set to 333kHz while the limit cycle is operated at a much lower frequency (fL) of 4,7kHz. The output of the transducer contains the pulse stream, which is the quantized low frequency input signal. This was converted into a parallel word by means of a up/down counter.

2. SYSTEM OPERATION

The digital current transducer is built using a ferrite core as the sensing element. The system is a closed loop limit cycling current control loop. The system contains a Schmitt trigger which provides the excitation signal for the toroidal core which has a rectangular B/H characteristic. The effect of this is to provide dither on the non-linear core which has been shown to provide a linearising effect[2,4].

The system is a zero flux system in that the limit cycle produces an offset current such that the mmf produced by the offset current is equal and opposite to the input current. This is observed as a Pulse Position Modulation (P.P.M) of the square wave produced by the limit cycle. If a Zero Order Hold (ZOH) is introduced into the system, it will result in a low order sigma delta modulator. The effect of this is to produce a digital transducer which can provide a

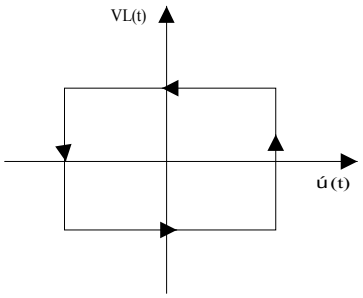

Fig. 2 Phase trajectory, between VL(t) and ú(t)

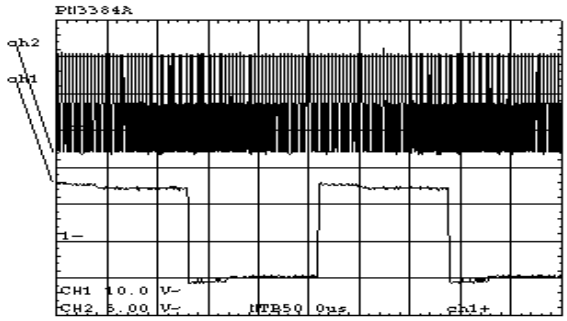

Fig. 3 Top trace Vc(t) of ZOH; bottom trace Vin(t) of drive amplifier

serial p.p.m output signal, decimation of which produces a digital word of n bit word. This can be achieved in the simple case by means of a up/down counter.

3. MATHEMATICAL MODEL

3.1 Analogue Output

A simple mathematical model of the analogue output can be derived by using the Kirchhoff mesh equation:

$$vin(t) = i1(t)R + \frac{d(L1(t)i1(t))}{dt} + \frac{d(M(t)i2(t))}{dt} \quad (1)$$

I1(t) is the exciting current through the current sense resistor and Vin(t) is the input voltage. In order to derive a valid model for AC and DC, it is assumed that the inductance L1(t) and L2(t) and the mutual inductance M(t) are time dependent due to the change of the relative permeability. The voltage drop across can then be estimated by :

$$vr(t) = R - \frac{1}{L1(t)} vin(t) + i1(t)R\,dt + \frac{N2}{N1} i2(t) \quad (2)$$

this can be further simplified to:

$$vr(t) = u(t) + \frac{N2}{N1} R\, i2(t) \quad (3)$$

where u(t) is the high frequency component of the limit cycle appearing at the output signal. If the voltage Vr(t) is passed through a low pass filter with unity gain, u(t) is removed and only the low frequency component remains. In this case Vr1(t) relates only to the low frequency components.

$$vr1(t) = \frac{N2}{N1} R\, i2(t) \quad (4)$$

3.2 Digital Output

The digital output Vout(t) will produce a P.P.M decimation which will provide the digital output signal which is passed through up/down counter. The value of the counter n depends upon the positive half cycle T1 and the negative half cycle T2. The value of the three digit counter n can be estimated by using the following relationship:

$$n = \frac{(T1 + T2)}{Ts} \quad (5)$$

where Ts is the period of the sampling frequency of the ZOH.

4.Limit Cycle Prediction

To create a limit cycle in the current transducer it is necessary to incorporate a Schmitt trigger as shown in Fig. 1. A phase portrait can be produced by the plotting voltage $v_L(t)$ and the flux linkage $ú(t)$. This results in the closed phase trajectory shown in Fig.2.It is well known that the inverse plot [1/VL(t)]vs. $ú(t)$ will provide an area which is proportional to time [5].The system can be described by using the relationship:

$$ú = \int_{t1}^{t2} u\, dt \quad (6)$$

In order to calculate the total period it is assumed that no offset and no input signal is apparent. This will result in the following approximation:

$$T_{tot} = \frac{4ú}{u} \quad (7)$$

where $v_L(t) = u(t)$ (8)

3. MEASUREMENT

Fig. 3 illustrates that with a zero input the pulse width of the negative and positive cycle of the amplifier voltage has the same duration. The top trace indicates the clock of the Zero Order Hold and the bottom trace shows the output voltage of the drive amplifier. Observation of the system with a dc input indicates that the pulse width of the negative and positive cycles changed respectively, Fig. 4. This results in a

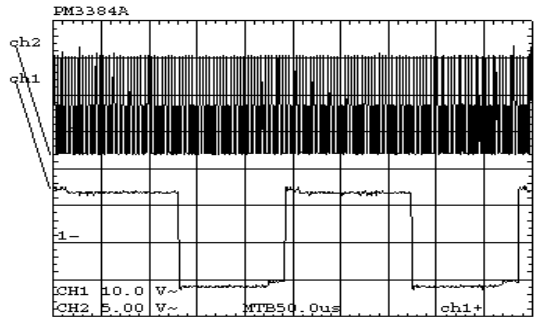

*Fig. 4 T*op trace Vc(t) of ZOH; bottom trace Vin(t) of drive amplifier

quantization of the dc input current $i_2(t)$, the ZOH provides the transition of the sampled amplifier output signal.

4.SIMULATION

4.1 Permeabililty

The use of the describing function method was not valid since there was not enough filtering in the system, shown in Fig. 5.

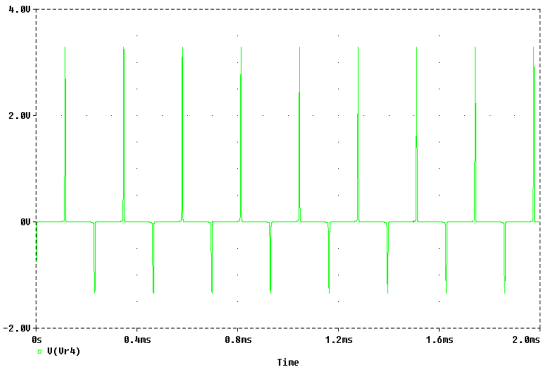

Fig. 5 voltage drop vr(t)

The modelling of the permeability is more complex since higher harmonics are transmitted through the system. Jiles-Atherton [6] suggested a method which described the magnetisation by the use of Langevin [7] function. The permeability was described to be :

$$\acute{c}\,r\ddot{I}t\eth \mathrm{I}\ddot{I}1\mathrm{M}\frac{dM}{dH}\eth \tag{9}$$

Since the new current transducer is operated in extreme saturation Fig. 6 it was learnt that the excitation signal produces a very large field strength within the core, so that the hysteresis effect can be neglected.

Measurements of these signals provided the prove that the hysteresis curve can be approximated by applying a Fast Fourier Transform (FFT). Table 1 shows the FFT results of the fourier coefficient of Vin(t) and Vr(t). These results were statistically analysed with MATLAB which resulted in a simplified expression, also mentioned in [8].

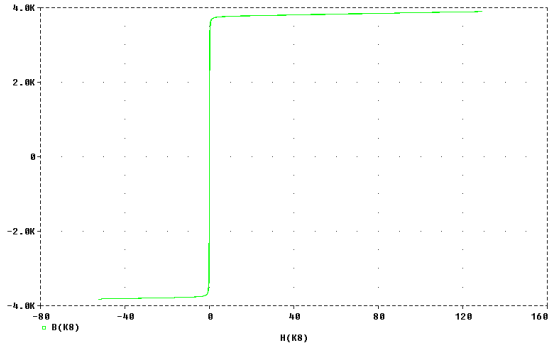

Fig. 6 Hystersis curve showing B(t) vs.H(t)with dc input i2(t)=10A

$$H\ \mathrm{I}\ Hc\ddot{I}arctanh\ddot{I}\frac{B}{Bsat}\eth\eth \tag{10}$$

At this instance the field strength H is derived by providing the coercive field strength Hc and the saturated flux density Bsat. The simulated hysteresis curve is shown in Fig. 6

Harmonic	*Input Vin(t)/V*	*OutputVr(t)/V*
1	15,000	1,000
3	5,190	0,530
5	2,900	0,350
7	0,000	0,250
9	0,000	0,180
11	0,000	0,135
13	0,000	0,097
15	0,000	0,075

Table 1 Fourier coefficent of Vin(t) and Vr(t)

4.2 Spice Simulations

PSPICE was used to perform simulations, PSPICE is an good tool to predict the highly non-linear systems. The ferrite core was simulated in the same manner as the analogue transducer with the Jiles Atherton model provided by the PSPICE Library [9]. Fig. 7 shows the simulated system with the dc input current and the

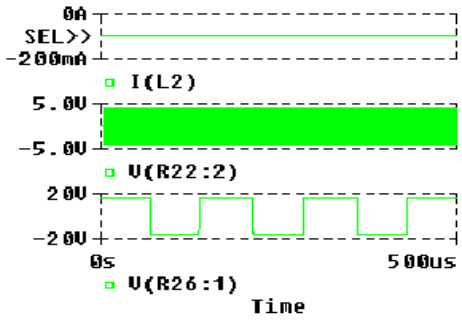

Fig. 7 Simulated system with dc input ;second trace Vc(t), bottom trace Vin(t)

other related signals such as the sampling frequency and the sampled limit cycle.

The typical output of the three digital decimal up/down counter for the dc input is shown in Fig. 8. It should be noted that the counter was designed in such a manner that it counted over one complete cycle before being reset, counting up on one half cycle and down on the next. The resulting integer number represents the actual dc input signal. It is required to detect the beginning of each limit cycle in order to obtain satisfactory reset and latch the output of the counter into a memory, Fig. 8. A comparison between

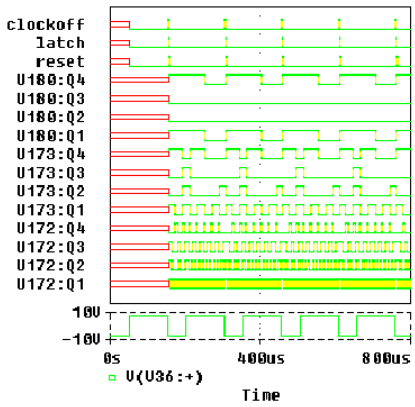

Fig. 8 Signals of the three digit up/down counter and trigger circuit

the digital output (n) and analogue Vr1(t) output shows a linear relationship. Table 2 shows the different dc input currents of the digital transducers. The results represent simulated values that the digital output produces at the up/down counter.

5.CONCLUSION

A new digital current transducer has been described which employs a non Hall sensing ferrite core. No DA conversion is necessary the bit length being limited by the sampling frequency in the bandwidth required. When the transducer is used in a system with harmonics above 1kHz, there is an improvement in the digital system, through the modification of the parameters necessary. As described in [2,3] a major improvement of the system can be achieved if a ferrite core with higher permeability is provided. It was seen that the height of the input amplitude is linked with the width of the modulation signal. If the user requires an adjustment of the input gain of the digital transducer, then this can be done by using a different resistor value and by changing the winding ratio. The bandwidth of the system is limited by the sampling frequency and the limit cycling frequency.

dc input current	3-digit-counter (BCD CODE)	Counter up/down	n=Counter values(Decimal)	n=Actual Decimal value	Vr1(t)
0.4A	0000.0010.0101	up	25	25	1
0.2A	0000.0010.0000	up	20	20	0,8
0.1A	0000.0001.0000	up	10	10	0,4
0A	0000.0000.0000	-	0	0	0
-0.1A	1001.1001.0000	down	990	-10	-0,4
-0.2A	1001.1000.0000	down	980	-20	-0,8
-0.4A	1001.0111.0101	down	975	-25	-1

*Table 2 D*ifferent dc input estimated with an up/down counter

6.REFERENCES

[1] Alexander Pross, T.Hesketh, A Limit cycling Digital Current Transducer, Sensors and their Applications X, IOP, 5-8 September 1999, pp.259-262

[2] Alexander Pross, Christopher Lewis, T. Hesketh, A Low Cost Analogue Current Transducer; Sensors and Actuators, accepted for publication, Elsevier Science, Nov.1998

[3] Alexander Pross, Christopher Lewis, T. Hesketh, A Low Cost Current Transducer, Eurosensor XII, 1998, pp.963-9

[4] Gelb A. and Vander Velde W., Multiple Input describing function,McGraw-Hill,1968

[5]Thaler a. Pastel, Analysis and Design of Non-linear Feedbach Control Systems, McGraw-Hill; 1962 ;pp.82-85

[6]Jiles, DC Atherton, Ferromagnetic hystersis,IEEE Trans. Magn.1(5)(1983),pp-2183-2186

[7]Jiles David, Magnetism and Magnetic Materials, 2nd Edition, Chapman and Hall,1998,p.138

[8]Gayle, F.Miner,Lines and Electromagnetic Fields for Engineers,Oxford University Press, 1996,pp.581-582

[9]MicroSim Corporation, Circuit Analysis Reference, 1997 Version 8.0